

P23G

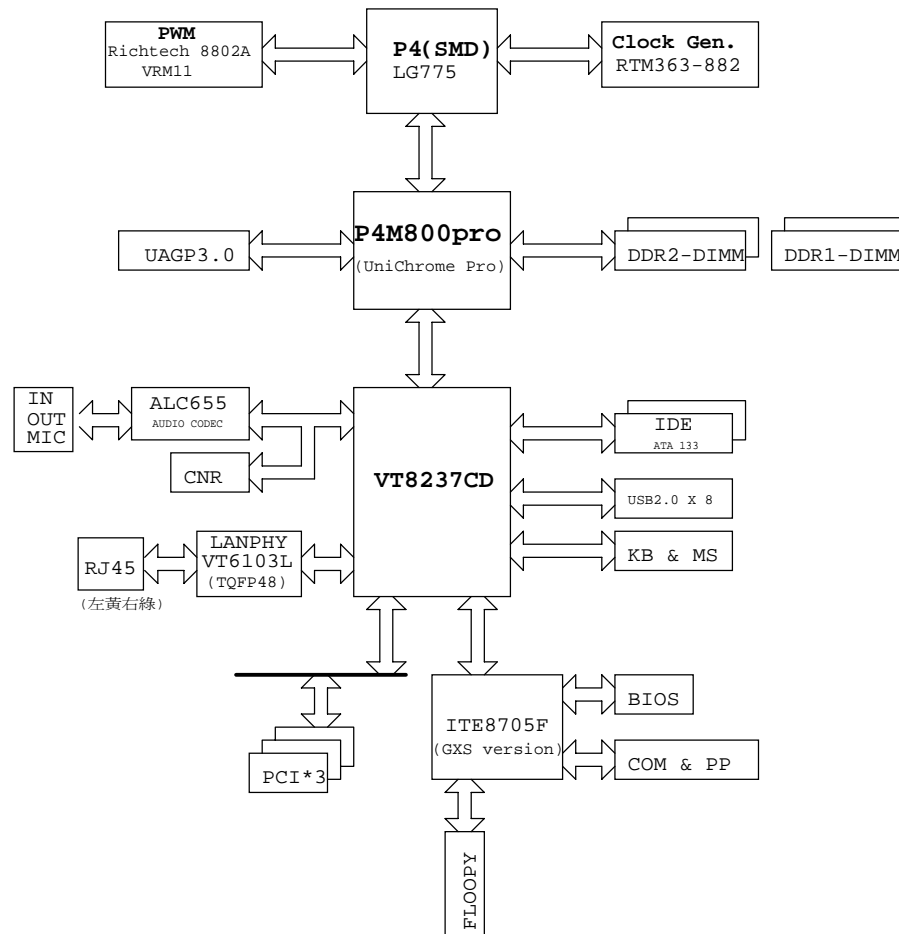
Rev :3.0

Schematics	PCB Ver.	BOM	Schedule			
	244*244*1.6 -2116		Schematics	Layout	Gerber Out	M/B return
A	15-N56-010010	89-200-N56000				
B	15-N56-010020	89-200-N56010	June/21/2005		July/8/2005	
C	15-N56-010030	89-200-N56020	Aug/5/2005	Aug/10/2005	Aug/17/2005	Aug/25/2005
D	15-N56-010040	89-200-N56030	Sep/27/2005	Sep/28/2005	Sep/30/2005	Oct/11/2005
1.0	15-N56-011000	89-200-N56100	Oct/21/2005	Oct/24/2005	Oct/25/2005	
3.0						

L2 : PWR
L3 : GND

Ver 3.0 Support CONROE, Using VRM11 PWM .

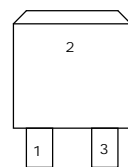
1	Cover Page
2	Block Diagram
★ 3	Clock Generator
★ 4	Power (CPU Vcore)
★ 5	Power (DC to DC)
★ 6	CPU P4-775(FSB)
★ 7	CPU P4-775(PWR, GND)
8	NB PM800pro (CPU)
9	NB PM800pro (MEM)
10	NB PM800pro (AGP , V-Link)
11	NB PM800pro (VGA)
12	AGP SLOT
13	SB 8237(PCI, USB)
14	SB 8237(IDE, GPIO, AC-Link)
15	SB 8237(V-Link, MII)
★ 16	Super IO(ITE8705F/FX,F/GX)
17	PCI 1, 2
18	PCI 3, CNR
★ 19	USB, PS2, IDE
★ 20	COM, LPT, VGA
21	AUDIO(ALC655), 6CH mute function
★ 22	Front Panel
★ 23	LAN PHY(VT6103L)
24	DDR II SLOT1
25	DDR II SLOT2
26	DDR I
27	DDR Terminator
28	VDIMM & DDR VTT



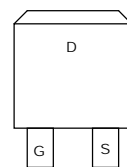
	Impedance	PCB 2116
USB_DT0+/-	(45/90)	8/8/8(47/87) 8/5/8(47/80 allegro) 7.5/7.5/7.5(50/90 guide)
LAN RX+/- TX+/-	(50/100)	8/8/8(47/87) 8/12/8(47/91 guide)
S-ATA	(50/100)	20/6/8/6/20(56/103) 17/6/8/6/17(guide) group mismatch 20 mil.
R.G.B	(37.5)	50/10/10/10/10/10/50 12/?/12/?/12(guide) Put 75 ohm on CON

PCI Bus Resource			
PCI1	AD19	INTA,BCD	REQ0
PCI2	AD20	INTB,CDA	REQ1
PCI3	AD21	INTC,DAB	REQ2

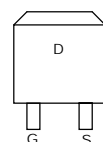
22U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



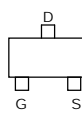
TO-263
B55QS03



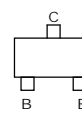
TO-263
2SK3296



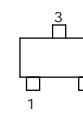
TO-252
20N03
TM3055TL-S
45N03
FDD6030L



SOT-23
2N7002
SI2303S
SI2301S



SOT-23
2N3904
2N3906
MMBT2907A



SOT-23
LM431
BAT54C
BAT54S



TO-92
LM431
78L05-D
LM432

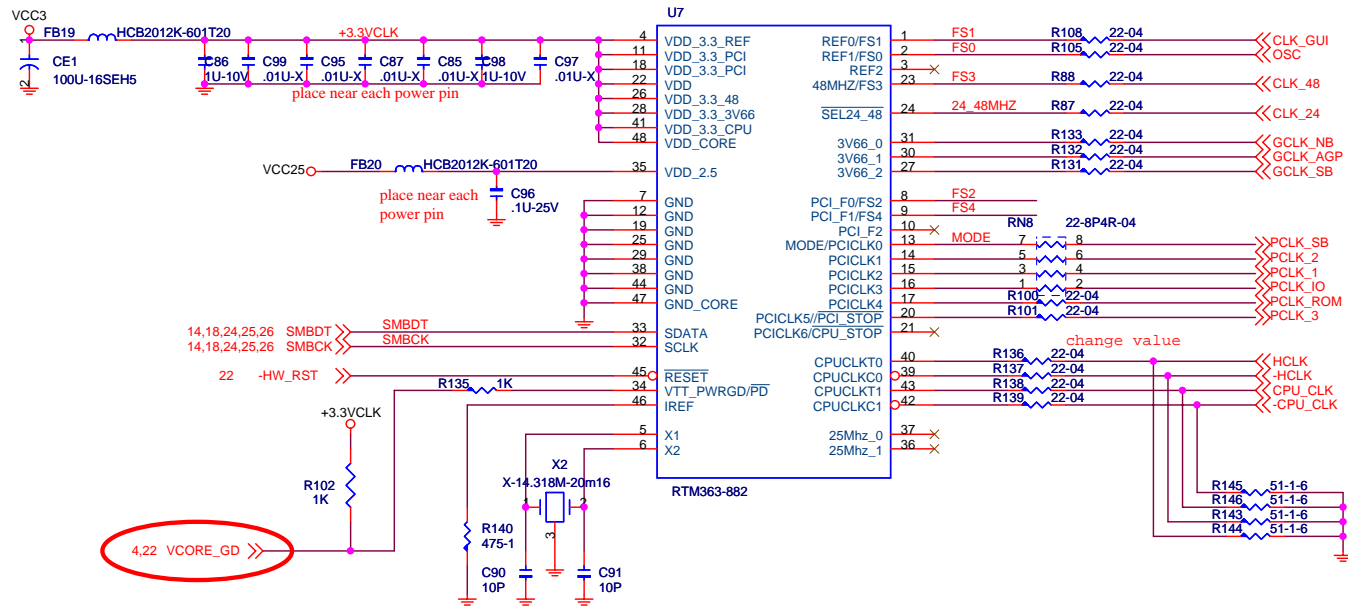


TO-92
2N2222A
2N2097A



TO-92
HSD882-D

Elitegroup Computer Systems			
Block Diagram			
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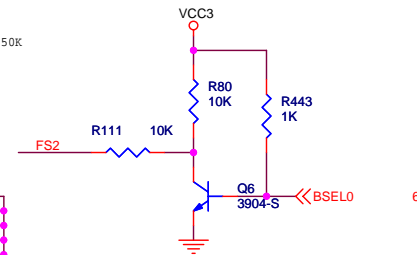
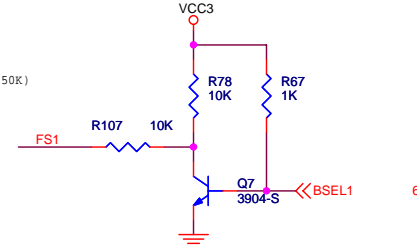


MODE R114 10K
Mode: Internal Pull-low 150K
For pin 20,21 PCICLK output

24 48MHZ R98 10K
Default (Internal Pull-low 150K)
Low: set to 48MHz
High set to 24MHz

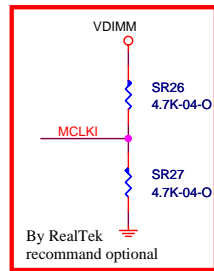
FS0 R109 10K
FS3 R99 10K
FS4 R103 10K
FS0,2,3,4: Internal Pull-low 150K

For EMI (Near CK GEN)
CLK GUI C318 1 2 10P-04
OSC C319 1 2 10P-04
CLK 48 C320 1 2 10P-04
CLK 24 C322 1 2 10P-04
GCLK_NB C321 1 2 10P-04
GCLK_AGP C323 1 2 10P-04
GCLK_SB C325 1 2 10P-04
PCLK_SB C324 1 2 10P-04
PCLK_IO C327 1 2 10P-04
PCLK_ROM C326 1 2 10P-04
PCLK_1 C328 1 2 10P-04
PCLK_2 C330 1 2 10P-04
PCLK_3 C329 1 2 10P-04



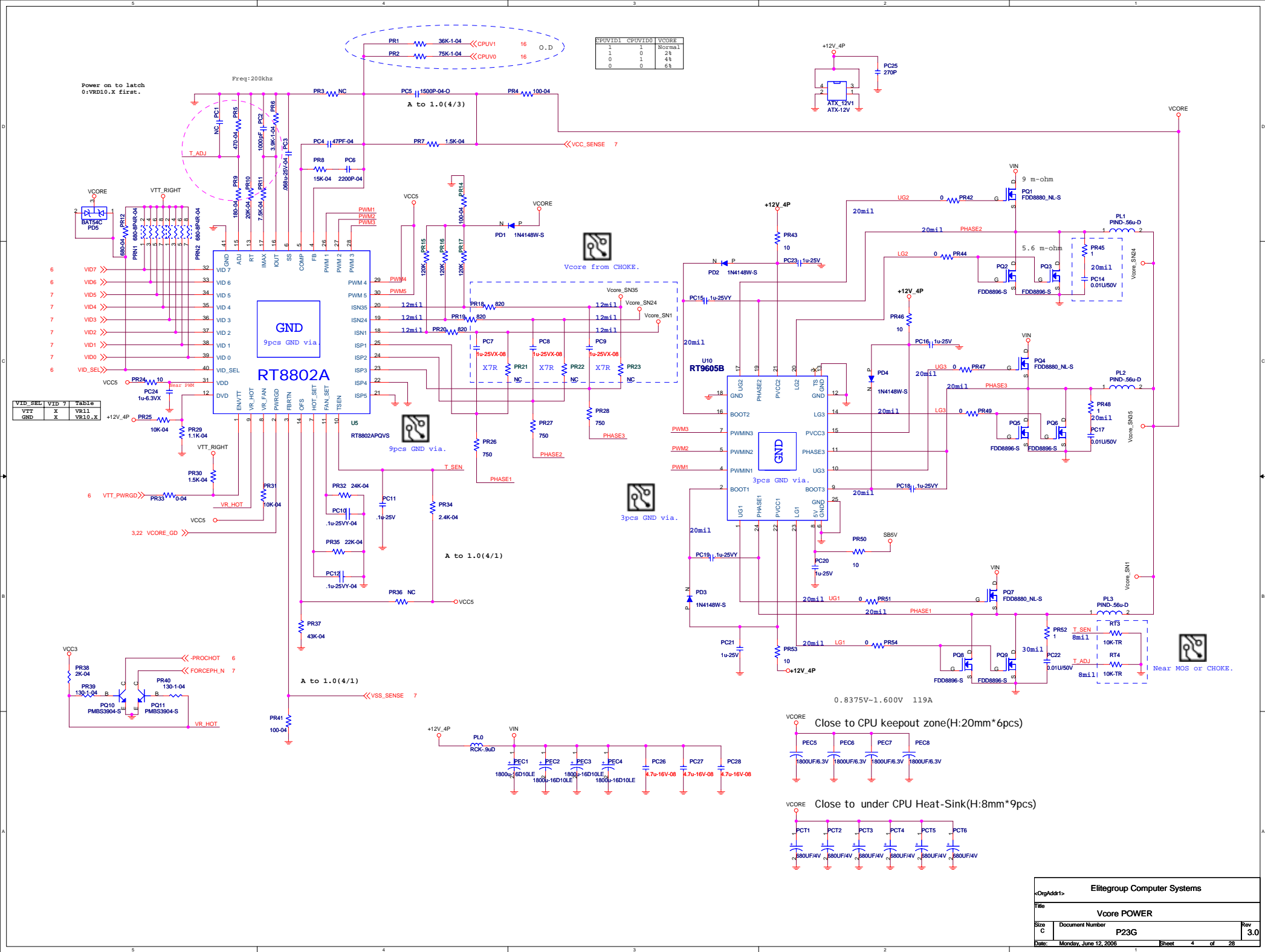
775CPU BESL					FS PIN			SB Strap
FSB		BSEL2	BSEL1	BSEL0	FS2	FS1	FS0	GPIOC
533	133	0	0	1	0	1	0	1=Auto
800	200	0	1	0	1	0	0	1=Auto
1066	266	0	0	0	1	1	0	1=Auto

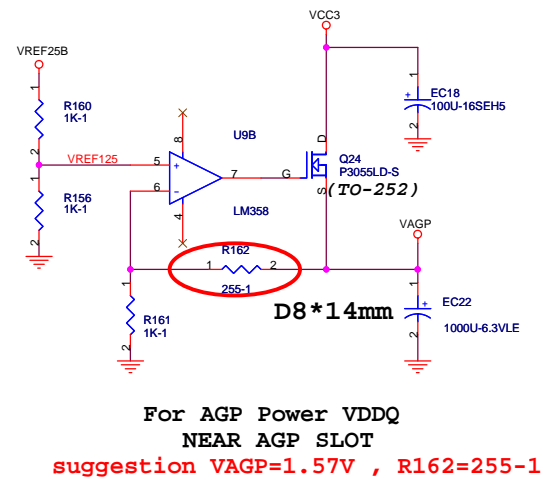
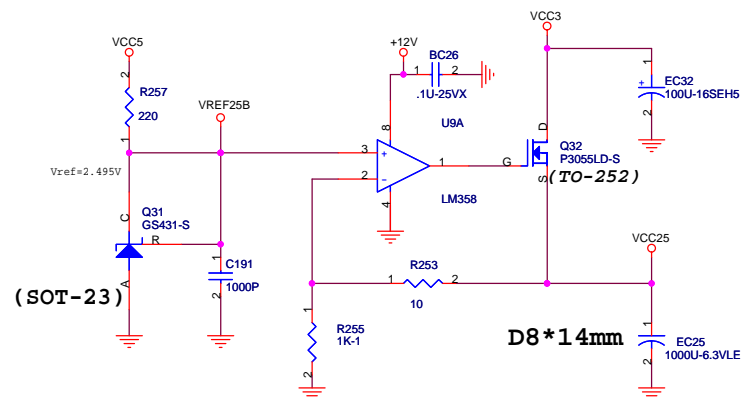
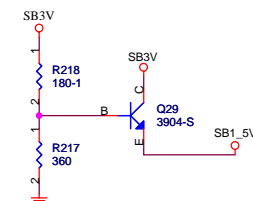
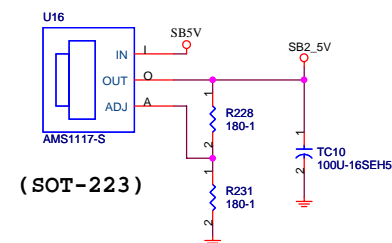
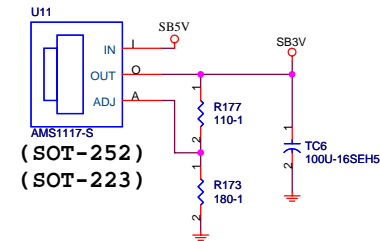
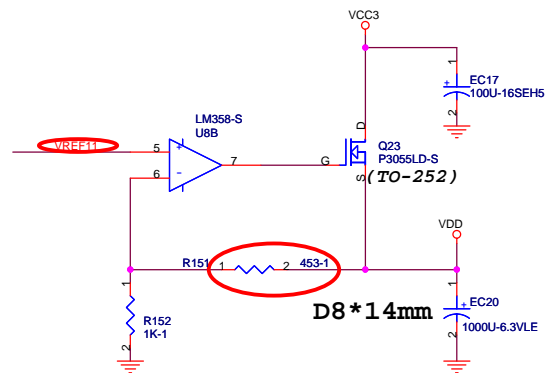
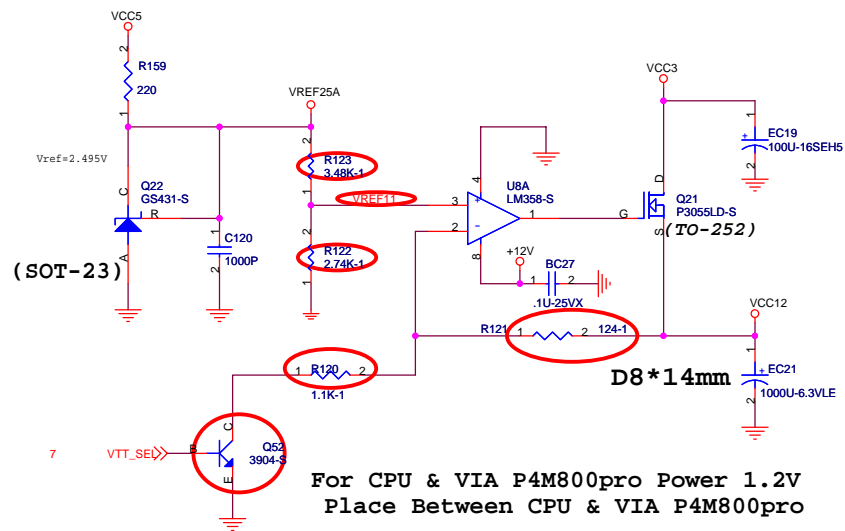
FS0 = Low;
FS1 = / BSEL1;
FS2 = / BSEL0;

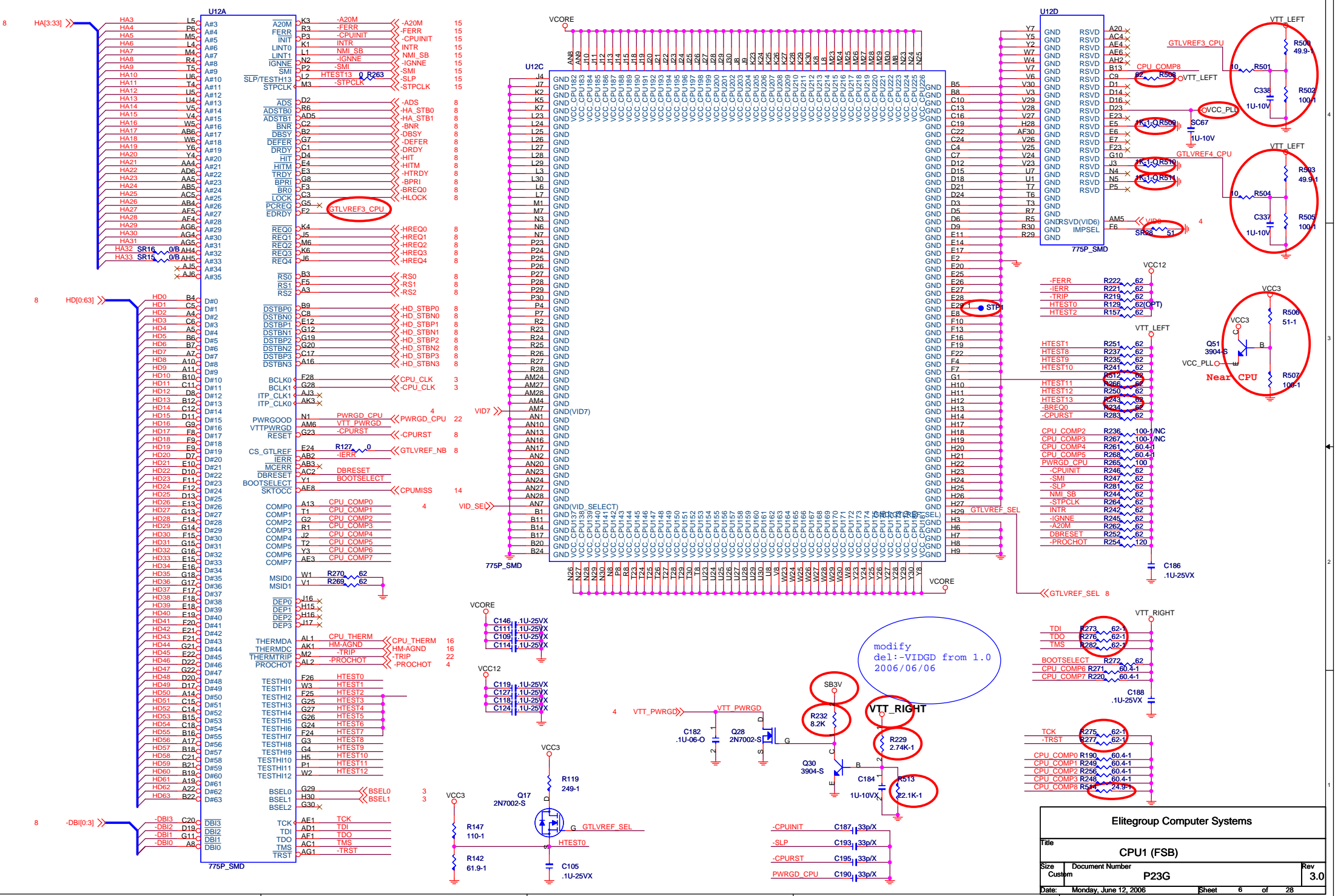


By RealTek recommend optional

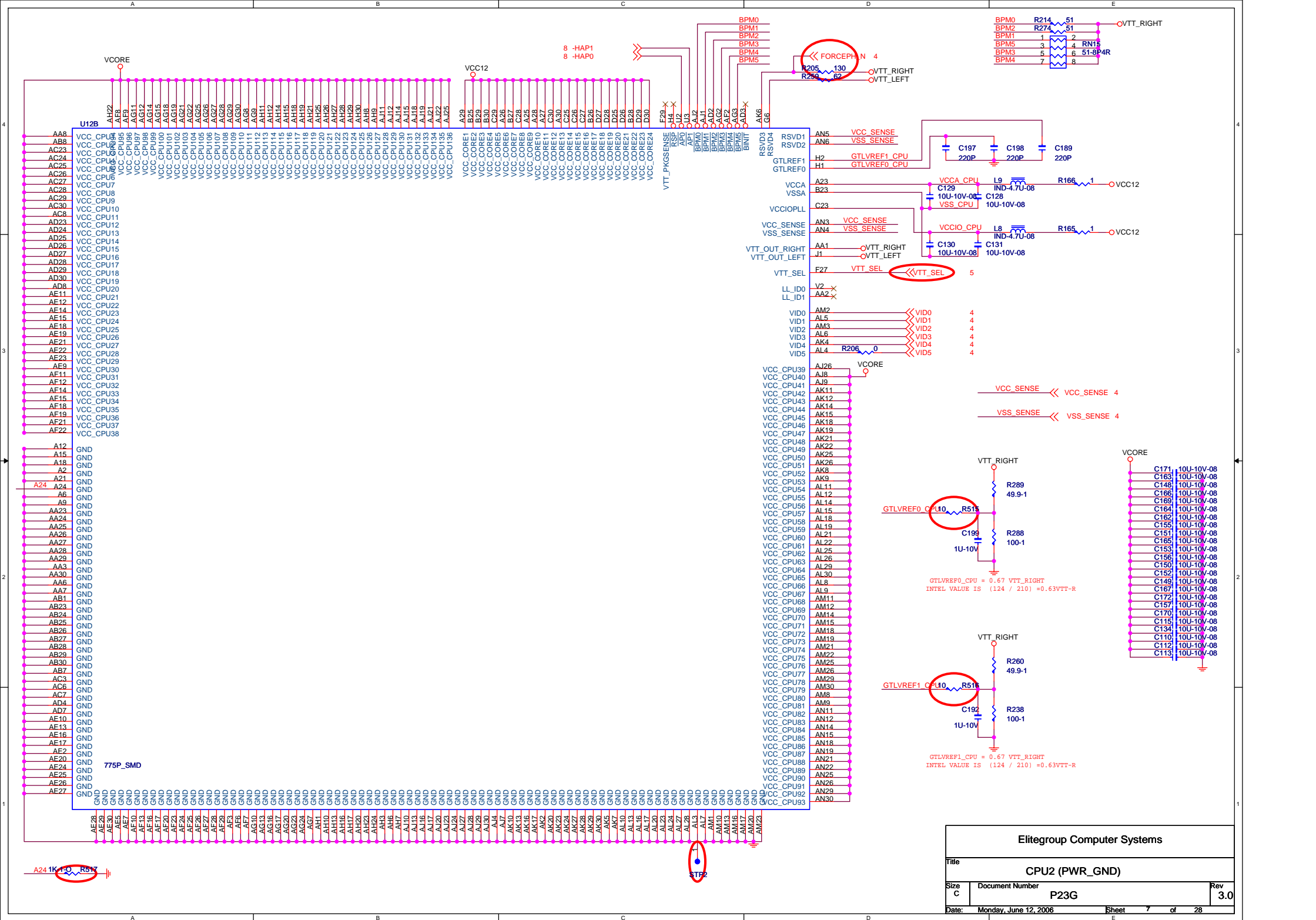
Elitegroup Computer Systems				
CLOCK SYNTHESIZERS				
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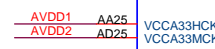
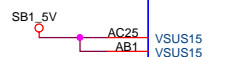
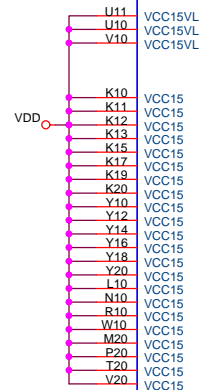
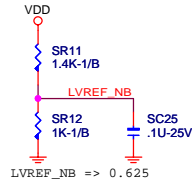
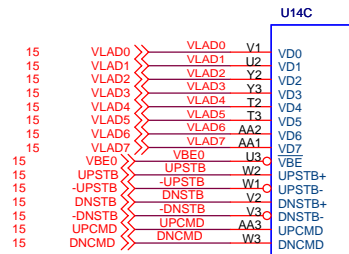
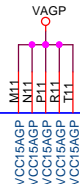
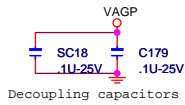




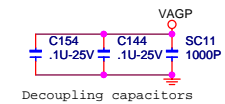
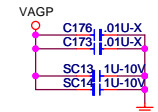
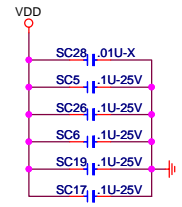
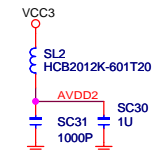
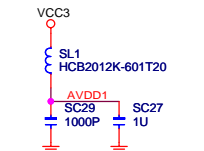
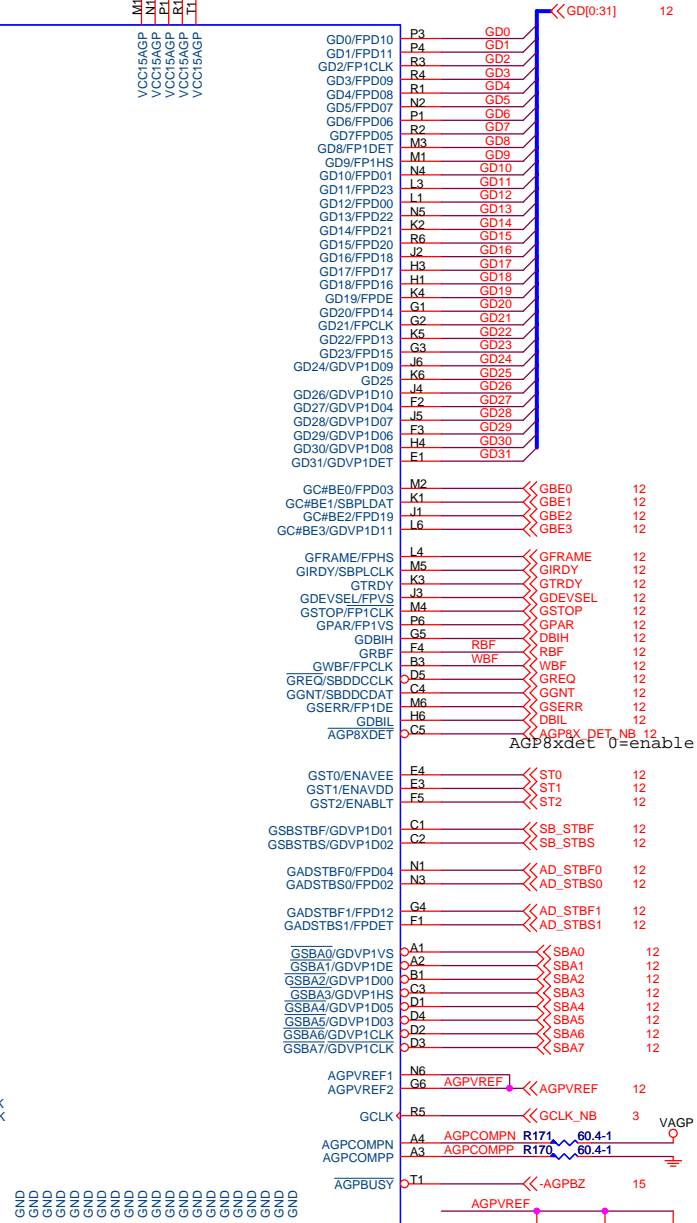


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Title			
CPU1 (FSB)			
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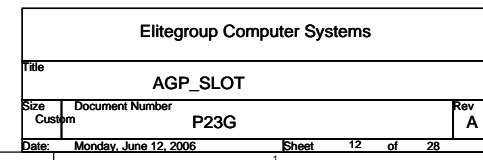


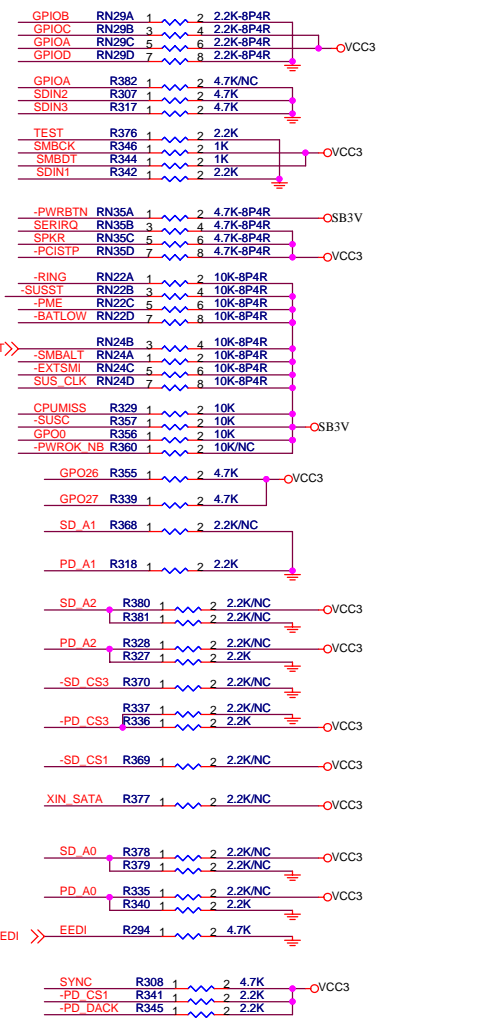
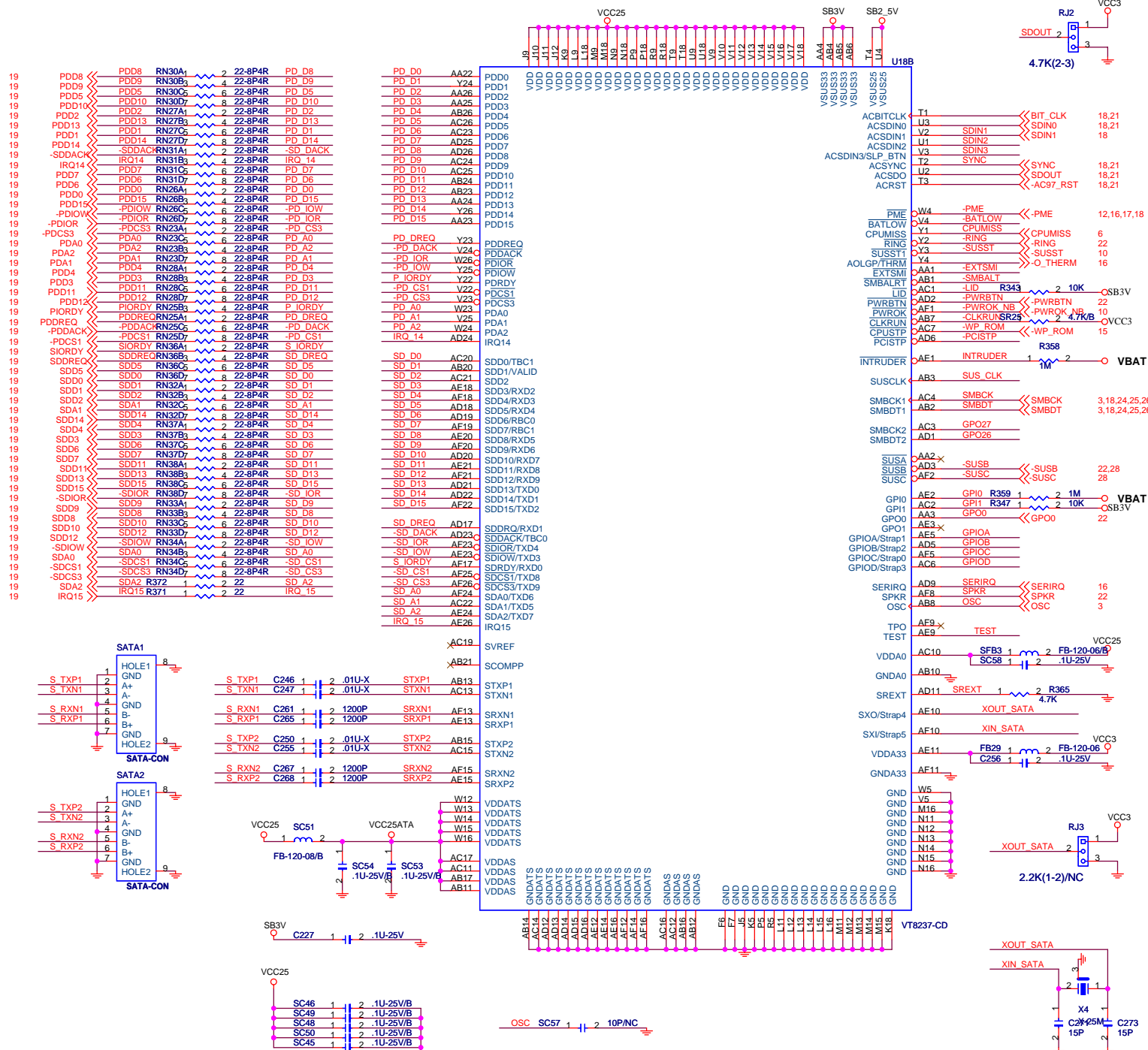
P4M800 Pro



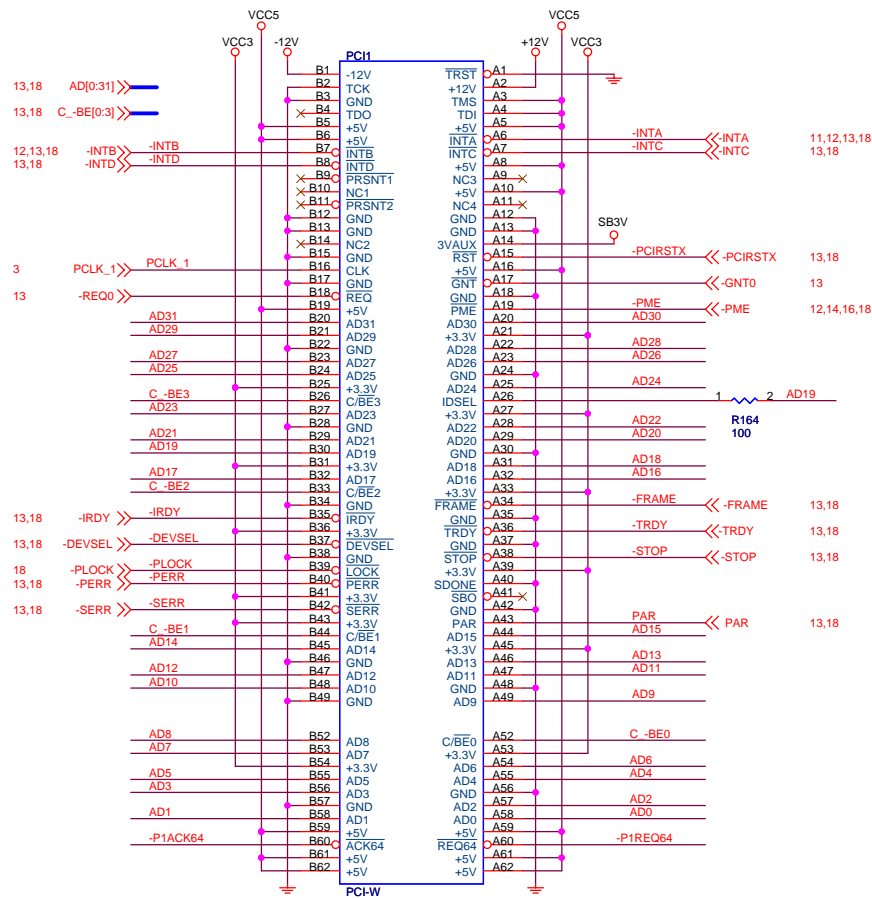
Strapping For NB_TEST Mode
TESTIN RBF WBF
1 x x Disable all TEST mode



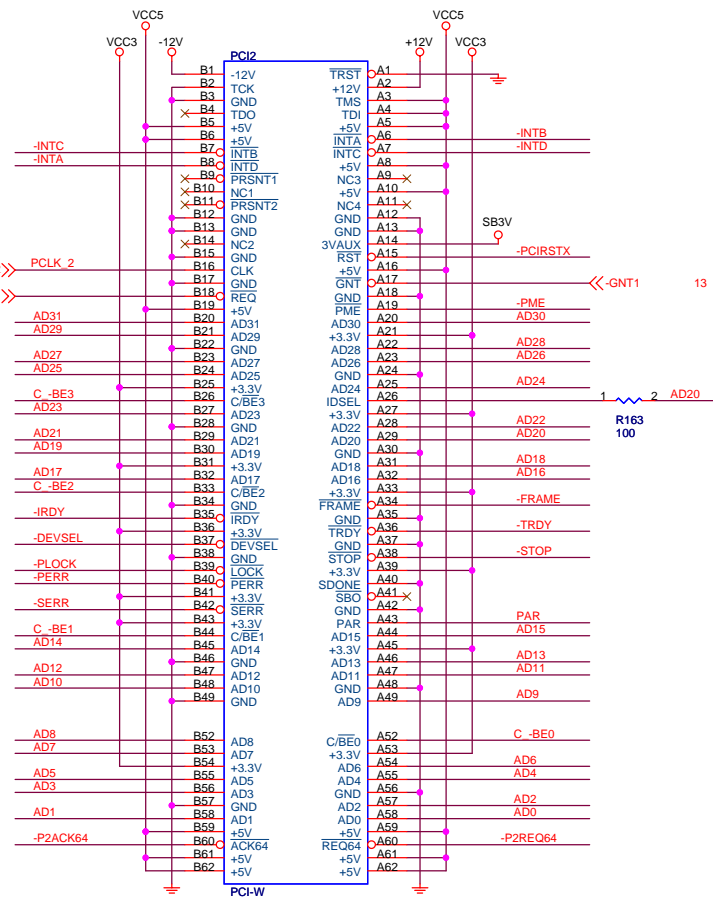
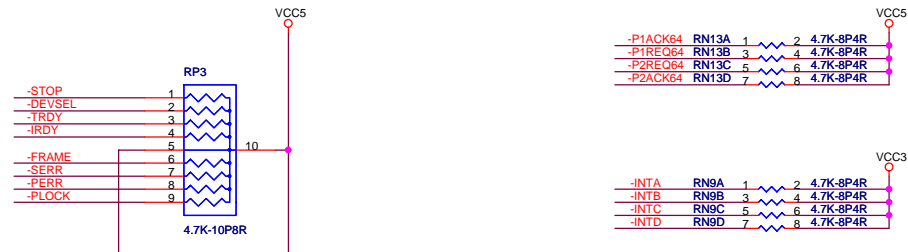




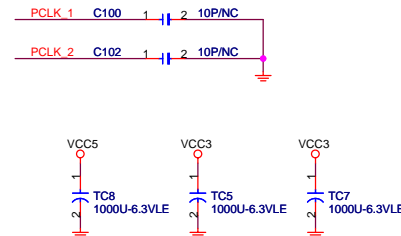
Elitegroup Computer Systems			
File SB (IDE_GPIO_AC-LICK)			
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INT:A
IDSEL:AD19

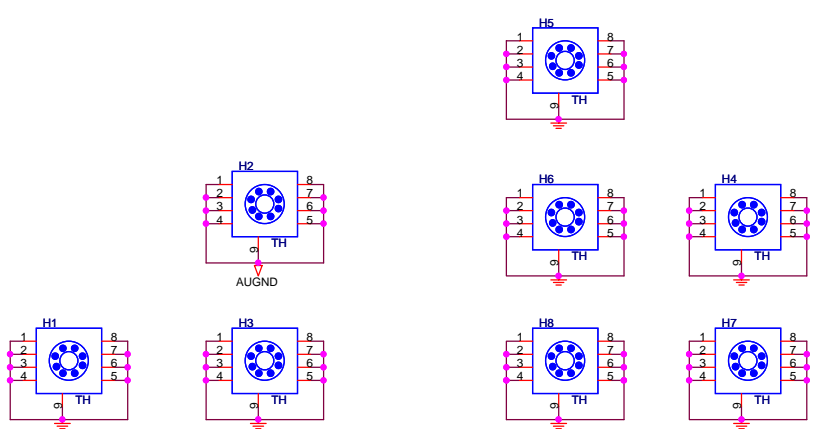
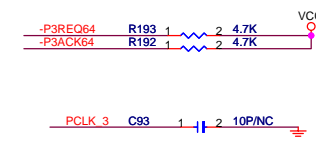
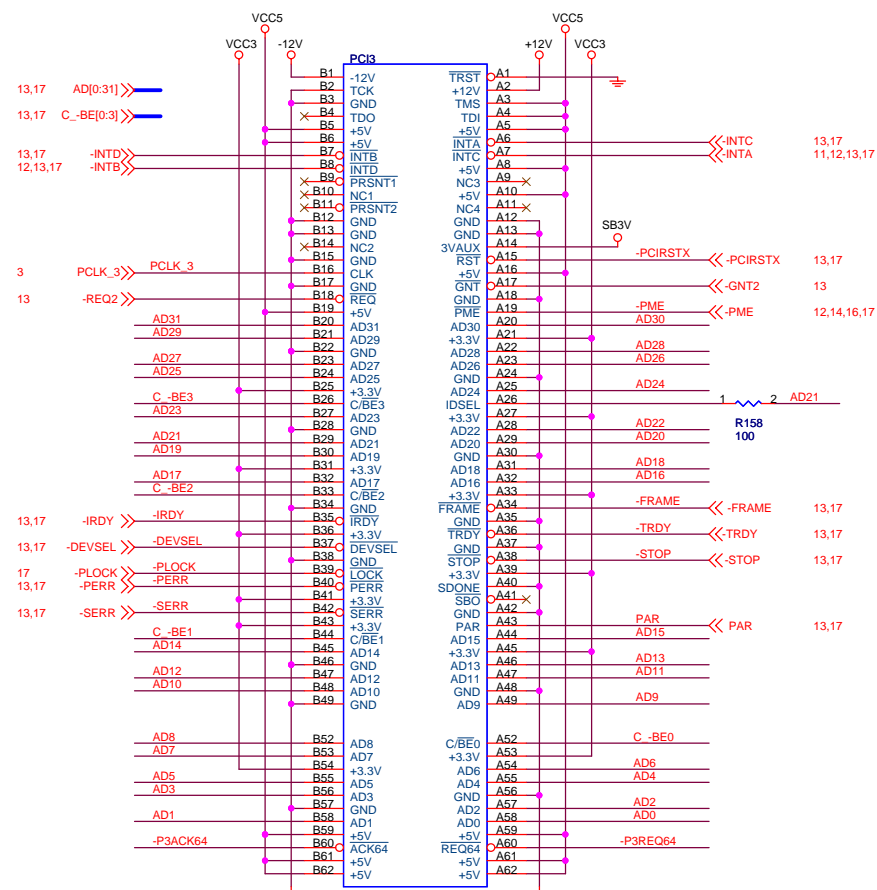


INT:B
IDSEL:AD20

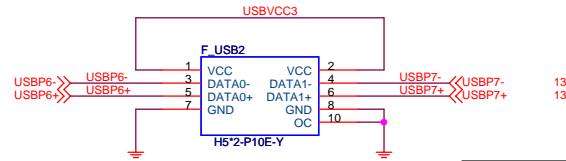
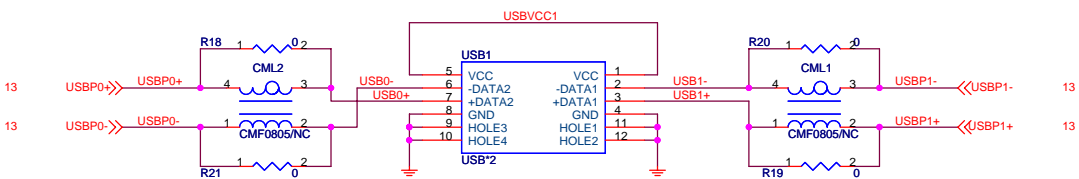
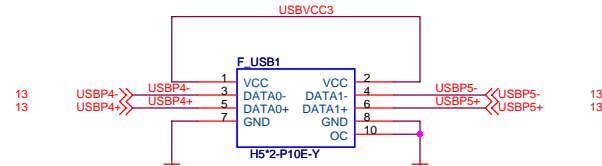
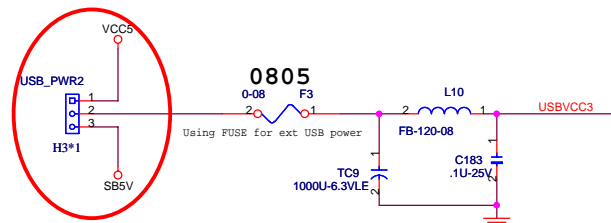
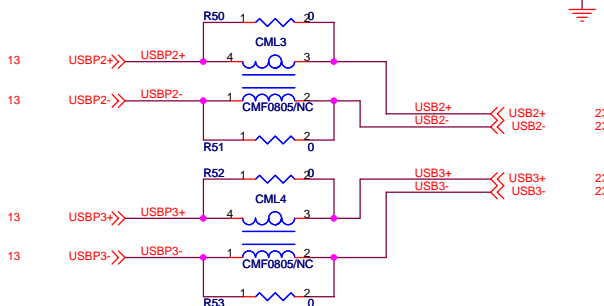
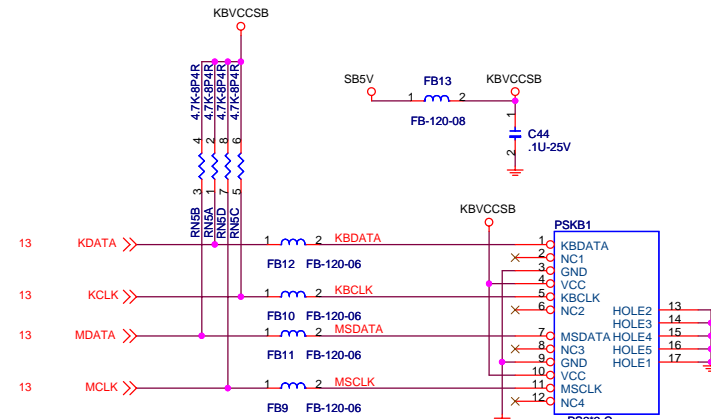
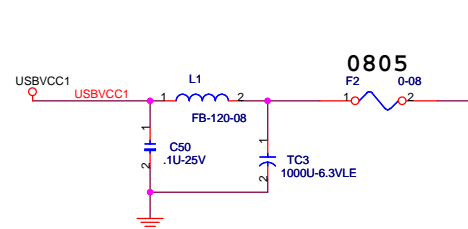
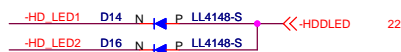
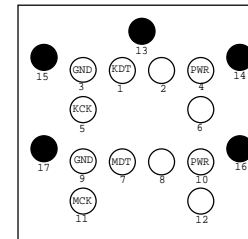
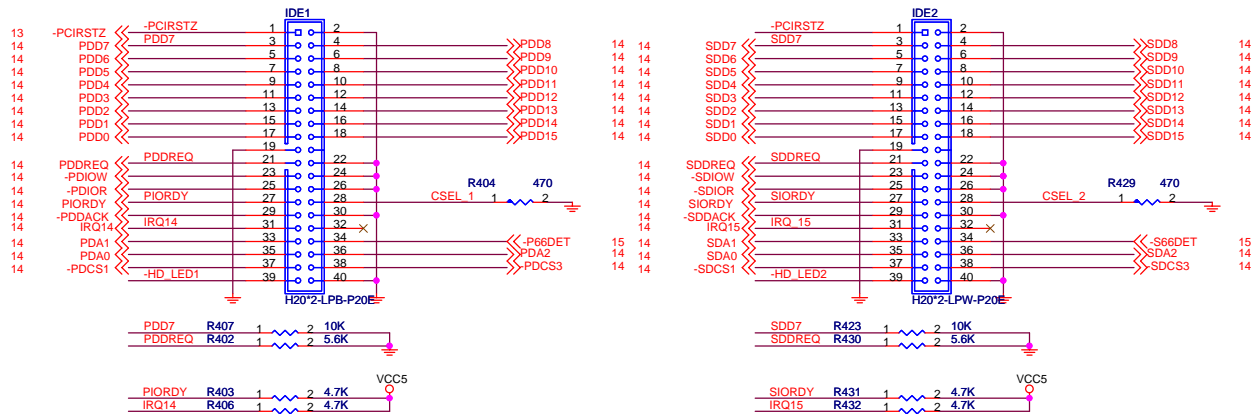


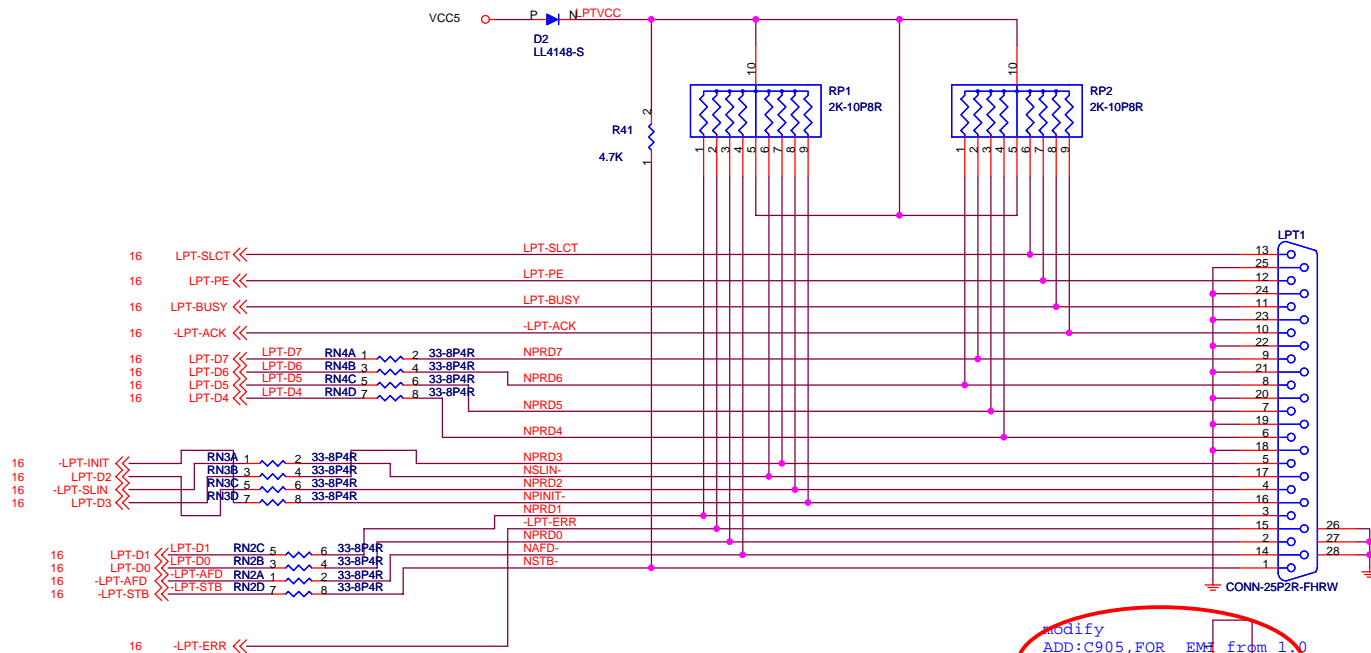
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PCI 3 & CNR			
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CP1,CP2,CP3,CP4 NC

LPT-SLCT 1 CP4A 2 180P-8P4C

LPT-PE 3 CP4B 4 180P-8P4C

LPT-BUSY 5 CP4C 6 180P-8P4C

-LPT-ACK 7 CP4D 8 180P-8P4C

NPRD7 1 CP3A 2 180P-8P4C

NPRD6 3 CP3B 4 180P-8P4C

NPRD5 5 CP3C 6 180P-8P4C

NPRD4 7 CP3D 8 180P-8P4C

NPRD3 1 CP2A 2 180P-8P4C

NSLIN- 3 CP2B 4 180P-8P4C

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NPINIT- 7 CP2D 8 180P-8P4C

NAFD- 1 CP1A 2 180P-8P4C

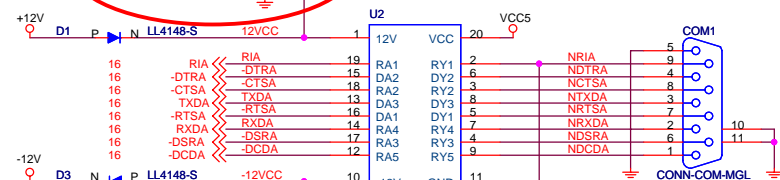
NPRD0 3 CP1B 4 180P-8P4C

-LPT-ERR 5 CP1C 6 180P-8P4C

NPRD1 7 CP1D 8 180P-8P4C

NSTB- 1 C43 2 180P

Modify
ADD:C905, FOR EMI from 1.0
2006/06/06



modify
ADD:C906, FOR EMI from 1.0
2006/06/05

TSSOP 20P

NRIA 1 CP6A 2 180P-8P4CF-O

NDTRA 3 CP6B 4 180P-8P4CF-O

NCTSA 5 CP6C 6 180P-8P4CF-O

NTXDA 7 CP6D 8 180P-8P4CF-O

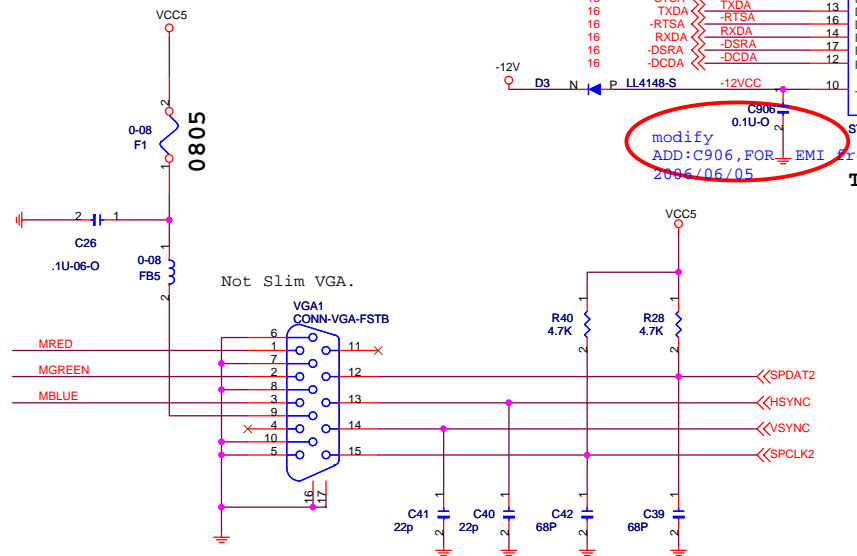
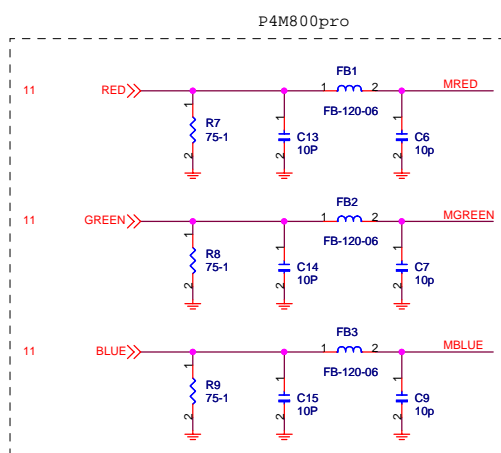
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NRXDA 3 CP7B 4 180P-8P4CF-O

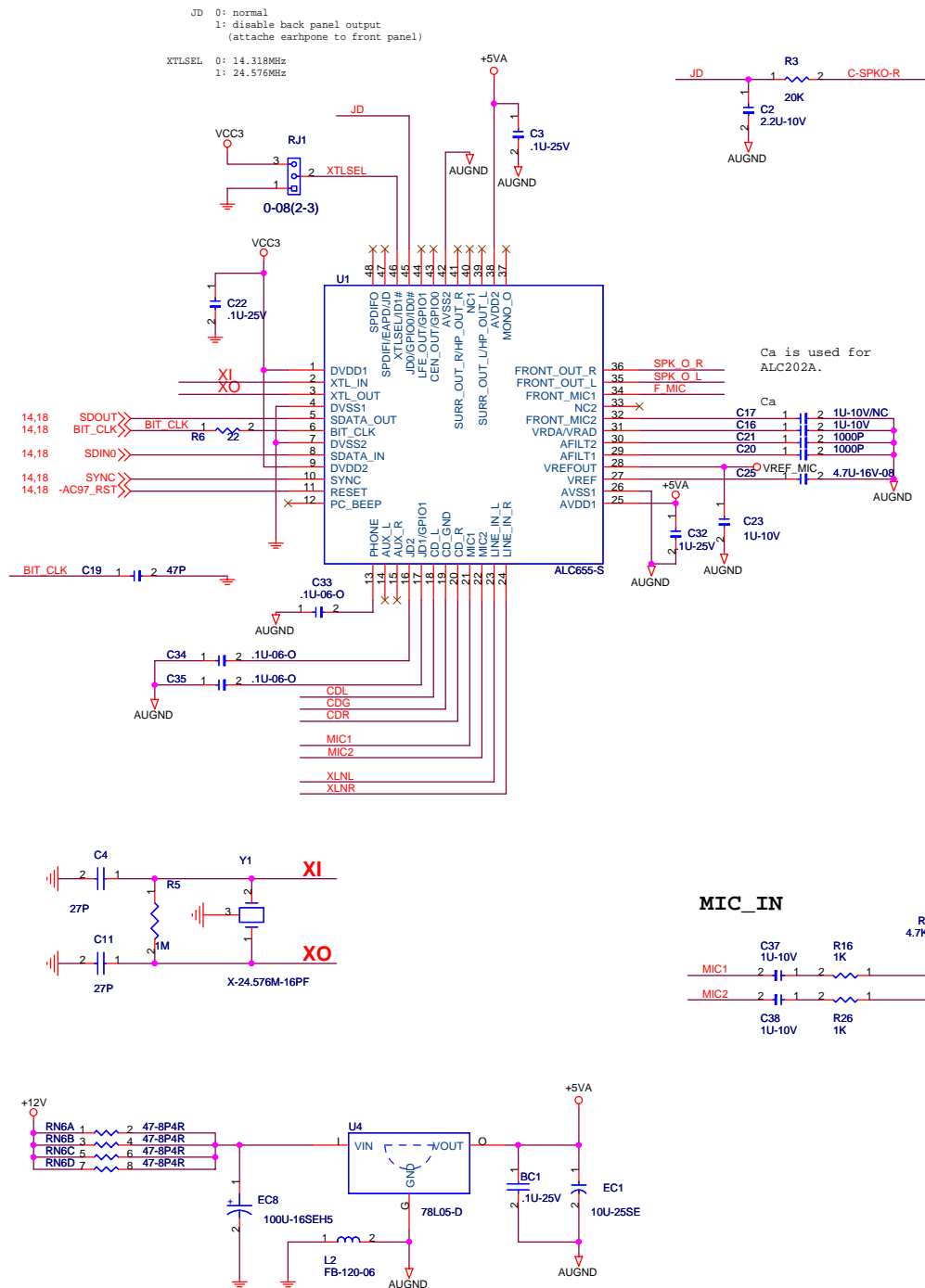
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NDCDA 7 CP7D 8 180P-8P4CF-O

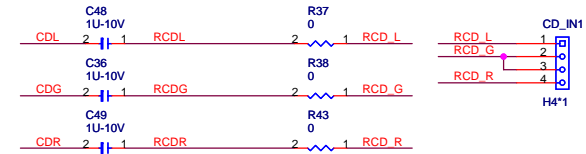
modify
ADD:CP6,CP7, FOR EMI from 1.0
2006/06/05



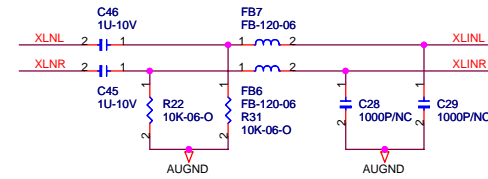
Elitegroup Computer Systems



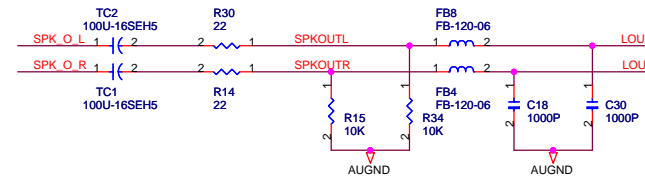
CD-IN



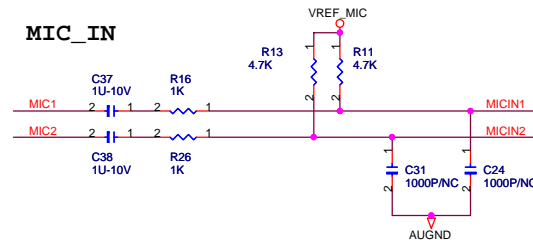
LINE_IN



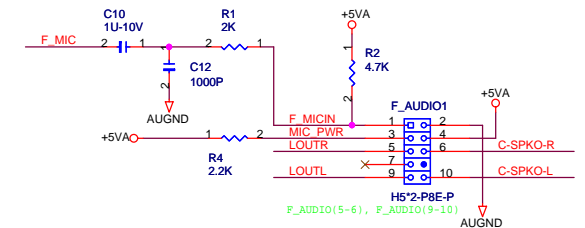
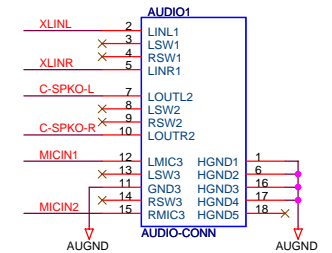
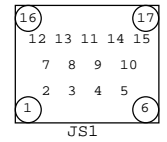
LINE_OUT



MIC_IN



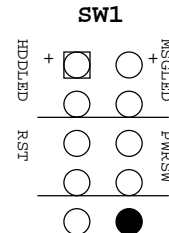
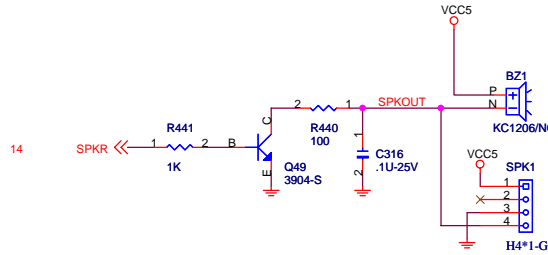
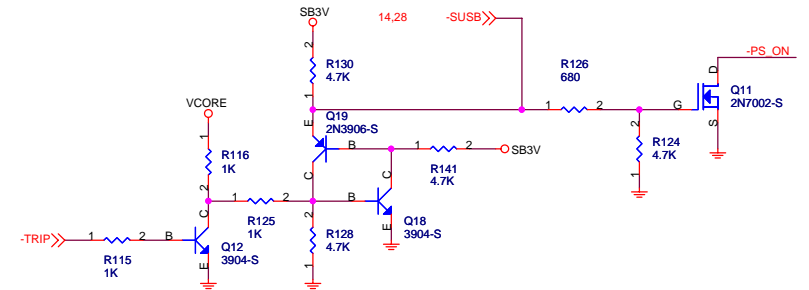
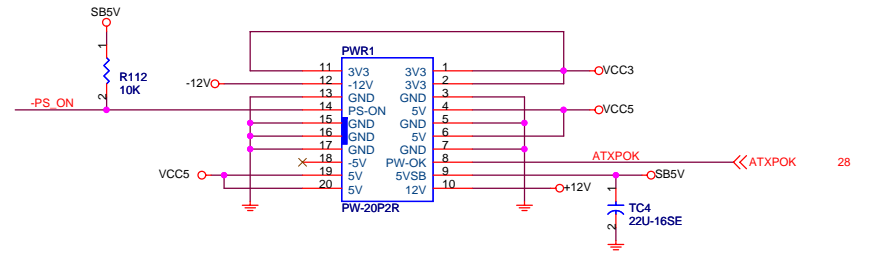
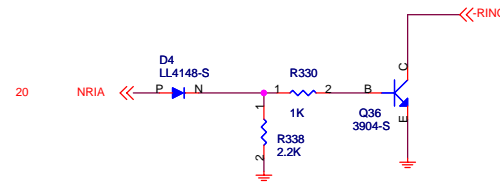
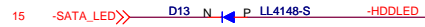
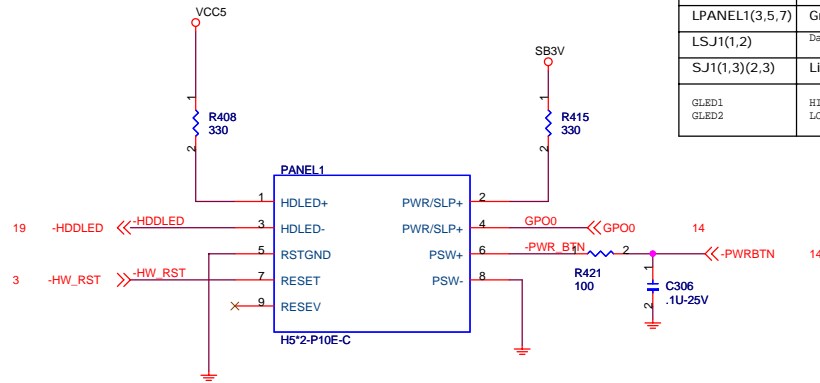
Top View



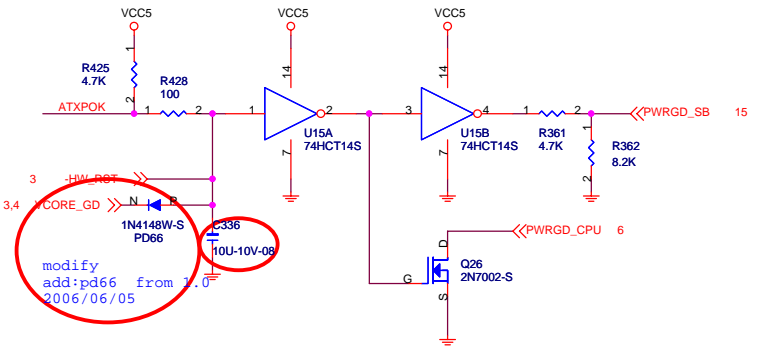
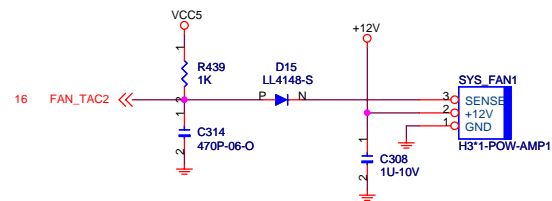
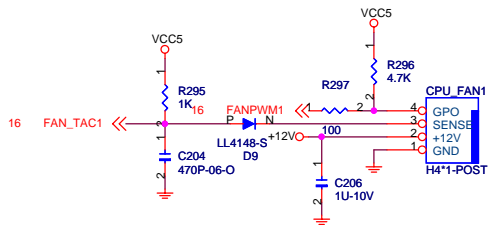
Elitegroup Computer Systems

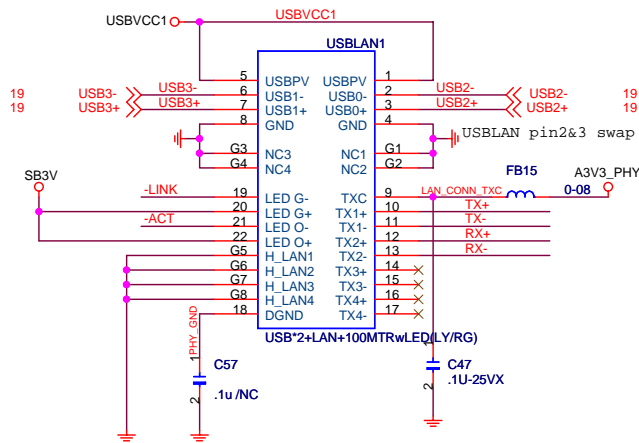
File			AUDIO
Size	Document Number	P23G	Rev A
Date:	Monday, June 12, 2006	Sheet	21 of 28

	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark Blinking	Light	Dark
SJ1(1,3)(2,3)	Light		Blinking	Dark
GLE1 GLE2	HIGH LOW	HIGH SWITCH	LOW SWITCH	HIGH HIGH



B to C(3/17)

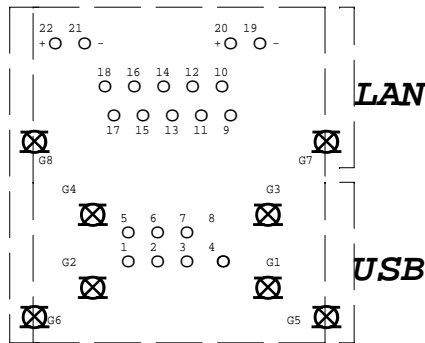




modify
ADD:R900,FOR EM1 from 1.0
NEAR USBLAN1
2006/06/05

	LED0	LED1	LED2	LED3	
00	LINK/ACT	SPEED	DUPLEX	COL.....	DEFAULT
01	PWR/TXACT	LINK/RXACT	SPEED	DUPLEX	
10	SPEED100	SPEED10	ACT	DUPLEX	
11	PWR/TXACT	LINK/RXACT	SPEED	COL	

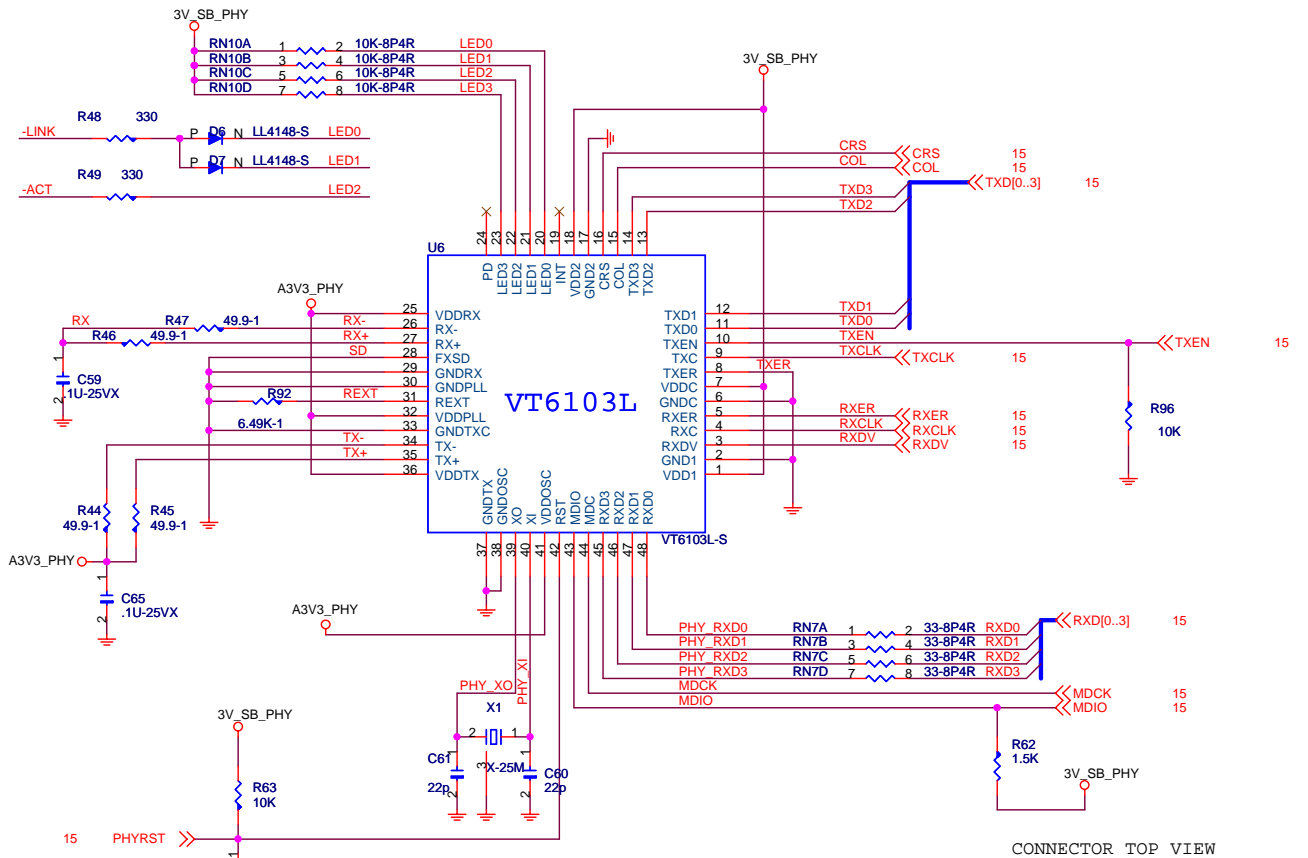
Yellow LED Green LED



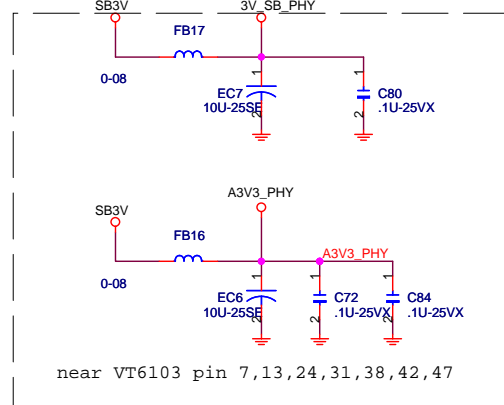
LNA CONN WITH TRSFOM
LED L-Y / R-G

10-084-022627

CONN.USB DUAL PORT+LAN.22P
90D.W/LED(LY-RG/O).10/100
TRANS LJ-H51SU3-52.LANKOM.

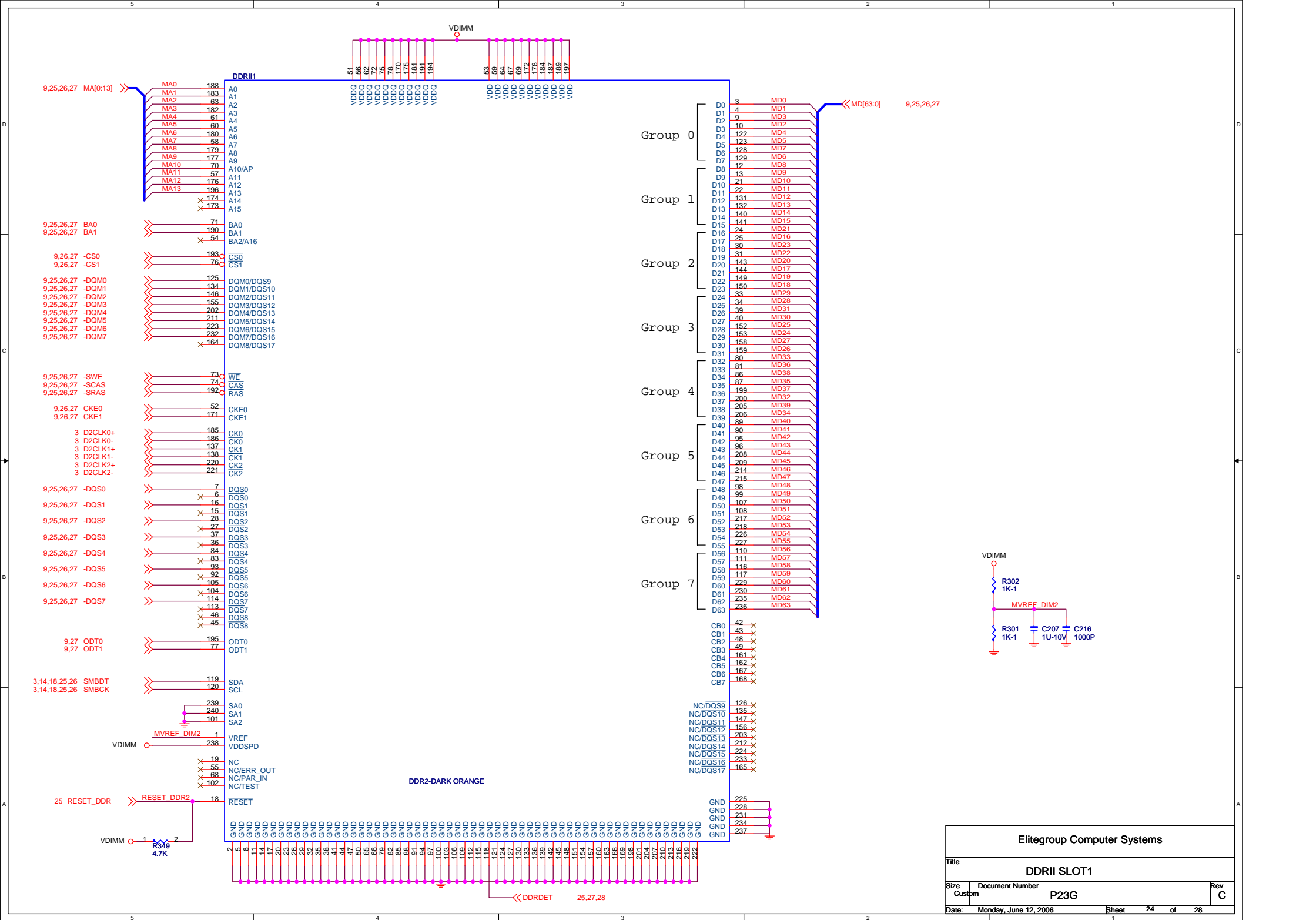


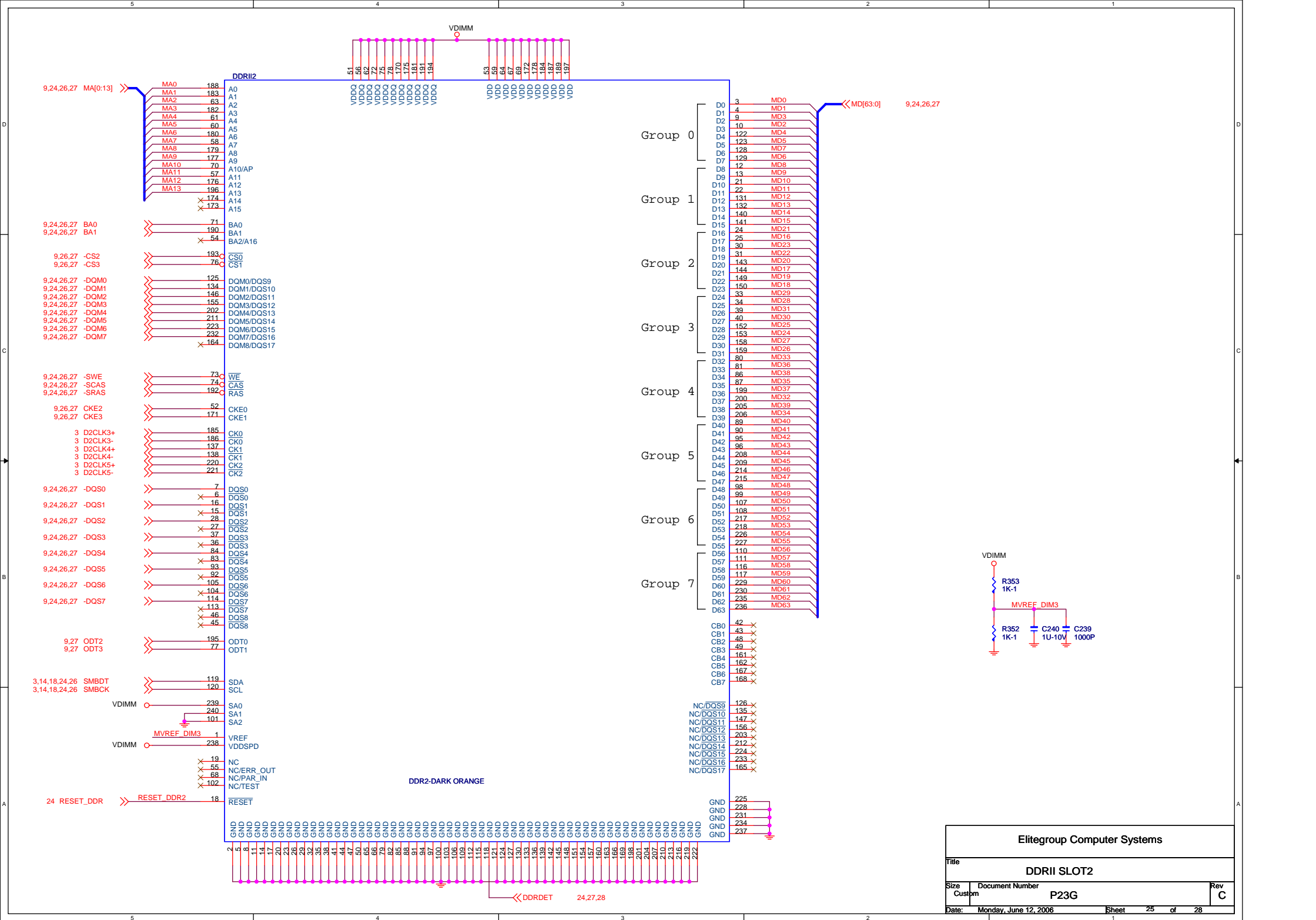
CONNECTOR TOP VIEW

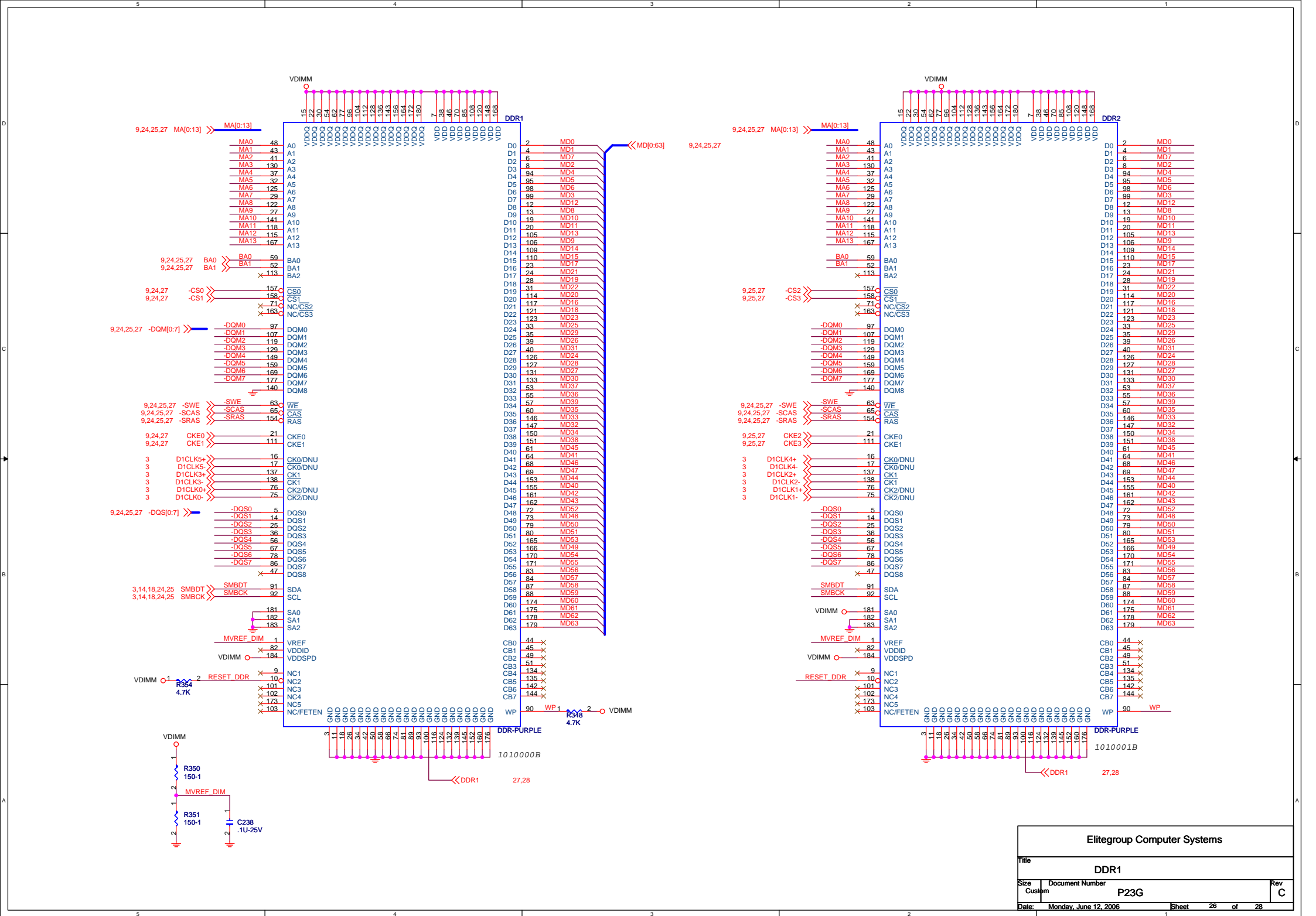


near VT6103 pin 7,13,24,31,38,42,47

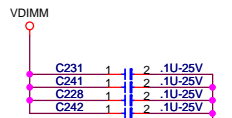
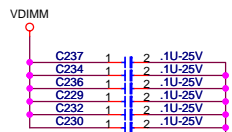
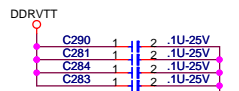
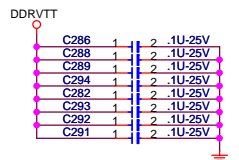
Elitegroup Computer Systems			
Title			
LAN (VT6103L)			
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9,24,25,26 MD[0:63] >> MD[0:63]
 9,24,25,26 MA[0:13] >> MA[0:13]
 9,24,25,26 -DQM[0:7] >> -DQM[0:7]
 9,24,25,26 -DQS[0:7] >> -DQS[0:7]

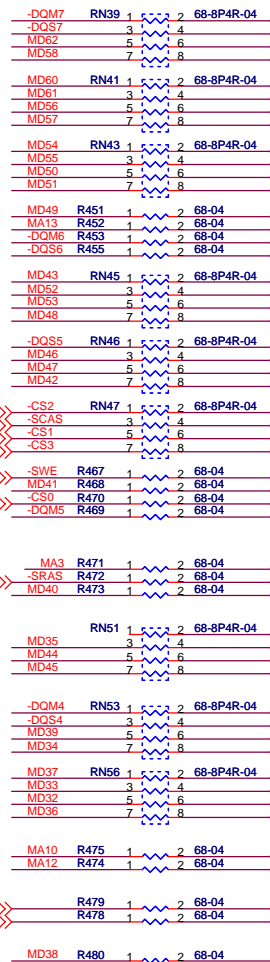


9,25,26 -CS2 >> -CS2
 9,24,25,26 -SCAS >> -SCAS
 9,24,26 -CS1 >> -CS1
 9,25,26 -CS3 >> -CS3
 9,24,25,26 -SWE >> -SWE
 9,24,26 -CS0 >> -CS0

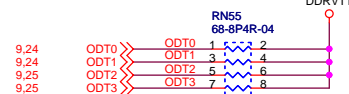
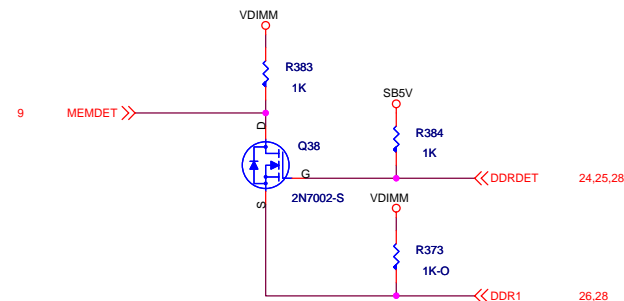
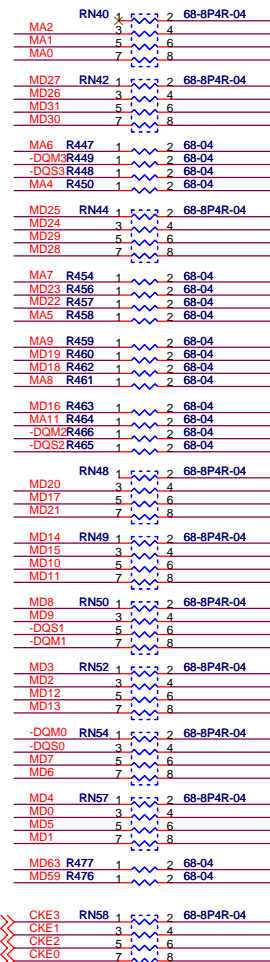
9,24,25,26 -SRAS >> -SRAS

9,24,25,26 BA0 >> BA0
 9,24,25,26 BA1 >> BA1

DDRVTT



DDRVTT



In order to improve DDR signals quality, we suggest to separate DDR signals to 4 groups:
 1.DQ/DQS/DQM
 2.MA/SRAS/SCAS/SWE
 3.CKE
 4.CS
 The different group signals should not share the same parallel resistor pack. It is also suggested to add decoupling capacitor for each parallel resistor pack.

